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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/523,385	02/01/2005	Johannes Otto Voorman	NL 020728	4142

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
LAMB, CHRISTOPHER RAY	
ART UNIT	**PAPER NUMBER**
2627	

MAIL DATE	DELIVERY MODE
06/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Interview Summary	Application No.	Applicant(s)	
	10/523,385	VOORMAN ET AL.	
	Examiner	Art Unit	
	Christopher R. Lamb	2627	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Christopher R. Lamb*. (3)_____.

(2) *Michael Scaturro*. (4)_____.

Date of Interview: *29 May 2007*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *1*.

Identification of prior art discussed: *Matsuda et al.*.

Agreement with respect to the claims f)☐ was reached. g)☒ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *See Continuation Sheet*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

William Korzuch
WILLIAM KORZUCH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

_____
Examiner's signature, if required

Continuation of Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: Applicant faxed a proposed amendment (attached). The Examiner indicated that the claim limitation wherein the sequential logic circuit output signal pairs were to "be supplied directly" to at least one analog adder/subtractor would overcome the previous rejection: in Matsuda Fig. 9, the sequential logic circuits are not supplied directly to the adder/subtractor. The attorney and the Examiner also discussed the "differential functionality" mentioned in the fax. The Examiner agreed that this functionality was present in the application, but noted that it was also present in Matsuda. One pair of the sequential logic circuits of Matsuda Fig. 9 detects delay-differences between falling edges, and the other pair detects the same for rising edges. The Examiner noted this was not stated very clearly in Matsuda, but the Examiner reached this conclusion after stepping through the sequential logic of the circuit diagram of Fig. 9. Regardless, however, the Examiner agreed the proposed amendment would still overcome the current rejection, but indicated that a new search would be necessary before reaching any conclusion about the allowability of the claim.

5/24/2007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Voorman, et al.		
Serial No.:	10/523,385	Group Art Unit:	2627
Filed:	February 1, 2005	Examiner:	Christopher R. Lamb
For:	Optical Disk System with Delaylineless Delay-Difference Detector		

INFORMAL COMMUNICATION – AGENDA FOR TELEPHONE INTERVIEW

Examiner Lamb
Office: 1 (571) 272-5264
Fax: 1 (571) 273-5264

Examiner Lamb:

Responsive to your request, attached find a proposed agenda, for our telephone interview scheduled for Tuesday, May 29th at 11:00 AM.

Applicant's Participants:

Michael A. Scaturro – Applicants Attorney

Agenda

1) A discussion regarding the 102 rejection of Claims 1 and 2 as being anticipated by Matsuda.

   (a) **STRUCTURAL DIFFERENCES** - Fig. 9 of Matsuda shows a difference detector 110 that is structurally configured to include combinational logic, which sources sequential logic, which in turn, sources additional combinational logic. In contrast, Fig. 2 of the invention illustrates combinational logic which sources sequential logic, which sources the analog adder/subtractor. (see proposed claim 1)

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(b) **DIFFERENT FUNCTIONALITY** - The sequential logic circuits of the invention are comprised of a **First Pair** of sequential logic circuits for detecting delay differences between rising edges and a **Second Pair** of sequential logic circuits for detecting delay differences between falling edges, as recited in Claim 2. It is submitted that the reference does not teach this feature. Reference is made to Col. 7 of Matsuda in support. By introducing a **First Pair and a Second Pair** of sequential logic circuits, using both kinds of edges, the influence of time-jitter is less compared to the situation where just one kind of edge is used (See Spec @ page 2, lines 30+). (see proposed claim 1)

2) A proposed change to Claim 1

1. (Proposed Amended) Optical disk system comprising at least one photo detector comprising several sub-detectors for detecting at least a part of said optical disk, said at least one photo detector generating detection signals in response to said detection, the optical disk system further comprising several circuits, each circuit having an input directly coupled to a respective output of one of said several sub-detectors for receiving said detection signals, said several circuits comprised of at least one amplifier for amplifying detection signals and comprising at least one slicer for slicing amplified detection signals, the system further comprising at least one delay-difference detector for detecting delay differences in sliced amplified detection signals, characterized in that said delay-difference detector is delaylineless and comprises combinatorial-logic circuits for receiving output signals from said several sub-detectors and for generating signal pairs to be supplied to one of a first pair or a second pair of ~~and~~ sequential-logic circuits, said sequential logic circuits generating sequential logic circuit output signal pairs to be supplied directly to at least one analog adder/subtractor for adding/subtracting said sequential logic circuit output signal pairs.

Kind Regards,
Michael A. Scaturro
Reg. No. 51,356